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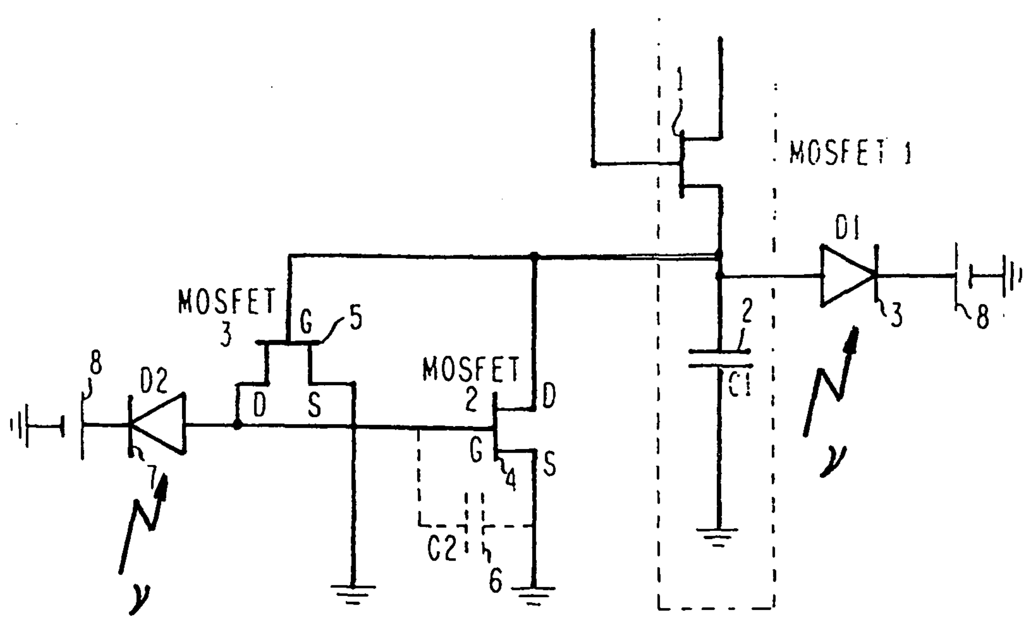
(54) Title: SINGLE ENDED THREE TRANSISTOR QUASI-STATIC RAM CELL



(57) Abstract: A single ended three transistor quasi-static RAM cell comprises two cross coupled MOS transistors and one select MOS transistor connected to drain of one of the aforementioned MOS transistors wherein drains of both cross coupled MOS transistors are each connected to anode of one of two PN diodes functioning as constant current loads when exposed to continuous light from LED diode.

WO 2004/084307 A1

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SINGLE ENDED THREE TRANSISTOR QUASI-STATIC RAM CELL

The cell has two stable states and and has only one port for data input/output.New solution is also introduction of light to PN junctions(diodes) which convert them in photodiodes . Photodiodes are constant current sources if exposed to continuous light .Furthermore it is object of this invention to show feasibility of manufacturing the memory cell using standard CMOS technology and occupying area of only four MOS transistors (3 active and one converted to two photodiodes).Power consumption of the cell in standby mode is small and it is only caused by photocurrent .

Figure 1 shows memory cell consisting of only 3 NMOS transistors , one select transistor and two cross coupled transistors . Instead of PMOS loads two PN (P+N) photodiodes , which normally have flat reverse I/U characteristic due to large dynamic resistance , are connected as loads to drains of cross coupled transistors . Memory cell (the whole chip) is exposed to low wavelength (red) light from LED diode glued on top of chip . Introduction of light to chip surface is not completely new . In UV EPROMs UV light is used to erase memory cells through window on top of chip .

However , static cell is operated (read and write) completely different from standard 6 transistor CMOS SRAM cell . It has only one select transistor thus it operate single ended .
Write and read operation are performed similarly as in one transistor dynamic RAM cell . Read operation is particularly interesting because current is sensed by sense amplifier rather than charge(voltage change) as in DRAM cell .Precharging is also necessary for bit line . Lower voltages (compared to Vdd voltage bias-5V or 3,3 V) are used for reading (1V for word line and 0,5 V for bit line for example) and if low threshold (Vgs=0,5 V) MOS transistors are used , reading is nondestructive as in static cell .In case of reading logical "1" small discharging (reading)drain current of select transistor will be compensated by photocurrent . In case of reading logical "0" charging (reading) drain current of select transistor (Ugs=1V and decreasing , Uds =0.5V and decreasing)is compensated by drain current of MOSFET 2 which comes immediately in saturation (Vgs = 5V and increasing Vds) .

Photodiodes are incorporated as P+ (anodes substitute drain/source function of PMOS transistor) in N well . Thus , memory cell occupy area of 3 NMOS transistor and 1 PMOS transistor . Technology for its manufacturing is 100% standard CMOS technology .
The only difference from standard 6 transistor CMOS static cell is that one select (NMOS) and one load (PMOS) transistors are removed .In remaining PMOS (load) transistor N well (N+) is connected to Vdd and P+ regions (drain and source) are connected to drains of cross-coupled NMOS transistors . When illuminated they function as load photodiodes .Metal contacts and poly(gate) are opaque to light which penetrates to P+ drain and source (photodiodes' anodes)region only , causing photocurrent , see fig. 2a .Light penetration of low wavelength (red) light in silicon is only 1 um which corresponds with shallow and thin P+N depletion layer .

Figure 2 shows chip cross-section incorporating classical CMOS inverter and figure 2a shows 2 NMOS transistors and two photodiodes connected as loads . Everything is technologycally identical except on fig. 2a N+ is connected (metalisation) to Vdd . It is possible because N+ is shaped in a ring while P+ are squares inside it .

Gate can be left floating or connected to Vdd .Since the PMOS transistors are enhanced mode (standard CMOS) it will not operate under zero (or positive) gate-source voltage .

Aforedescribed memory cell can operate in pulsed mode . Light source can be pulsed to save energy and information will not be lost because it will be kept dynamically between two light pulses .LED diode (red) which is necessary for light input (bias) is cheap compared to the price of memory chip .

In the CMOS process , after gate oxide growth , it is preffered that the poly layer (gate) should not be deposited on P channel transistor thus leaving large transparent area for light penetration in the N well . This significantly increases photodiodes' photocurrents particularly in relation to parasitic-unwanted photocurrent which is generated in drain (N+)-substrate (P) junctions of active NMOS transistors .

It is preffered that voltage difference between word line and bit line (precharge) in reading is equal to (low) threshold voltage of (enhancement mode) NMOS transistors . Light should be scaled to generate photocurrents in photodiodes equal to drain current of NMOS transistors in saturation (Vgs = Vthreshold , Vds = Vcc) .

It is possible to use standard sense (differential) amplifier which sense voltage difference between precharged bit lines because small current flow from or to the cell will slightly change voltage on connected bit line . Cell voltage (data) will not be changed . However , it is possible also to use current sense amplifier for direct sensing of read current .

What is claimed is :

1. A single ended three transistor quasi-static RAM cell comprising : two cross coupled MOS transistors and one select MOS transistor connected to drain of one of the aforementioned MOS transistors wherein drains of both cross coupled MOS transistors are each connected to anode of one of two PN diodes functioning as loads .

2. The device of claim 1 further comprising a light source optically coupled to PN diodes , said PN diodes generating constant photocurrents due to large dynamic resistance .

3. The device of claim 2 wherein light is generated by large light emitting diode optically coupled to RAM memory chip containing aforementionrd RAM cells , said light emitting diode being operated in preferably constant or pulsed mode .

4. The device of claim 1 wherein reading is performed by precharging bit line of select transistor to low voltage and word line to voltage larger for at least value of aforementioned MOS transistor threshold voltage causing small positive or negative drain current of aforementioned select transistor without changing output voltage level of cross coupled transistors representing stored data , said stored data being represented during reading by direction of drain current , said drain current being detected by current or voltage sense amplifier .

5. The device of claim 1 being manufactured by standard CMOS technology , said device being physically diferent from standard CMOS memory cell by not having one select NMOS transistor and one PMOS load transistor .

6. The device of claim 1 wherein total capacitance connected to drain of cross coupled MOS transistor connected to select MOS transistor is larger than total capacitance connected to gate of the same cross coupled transistor .

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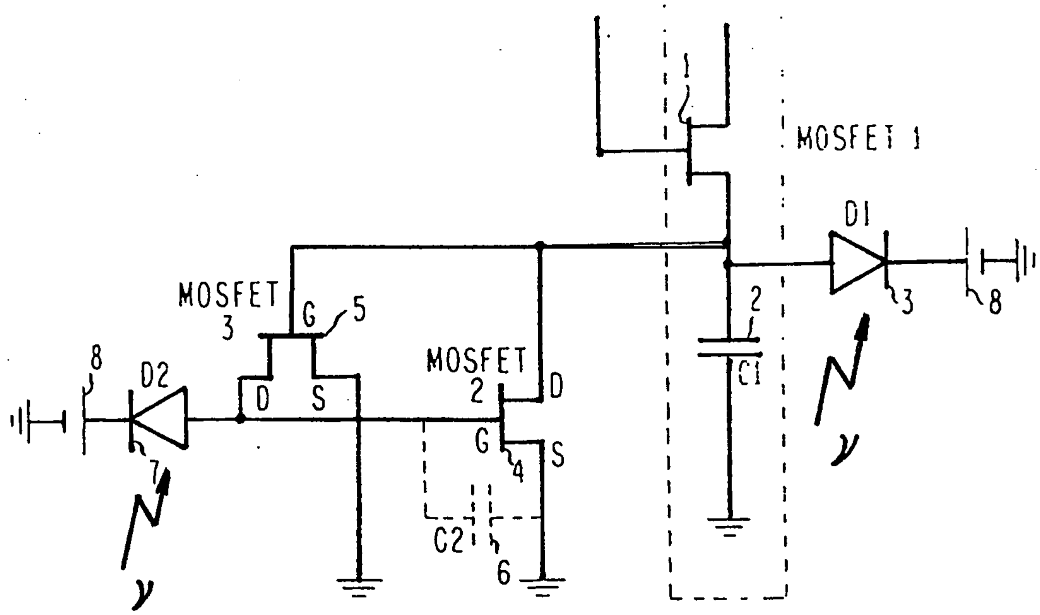

FIG. 1

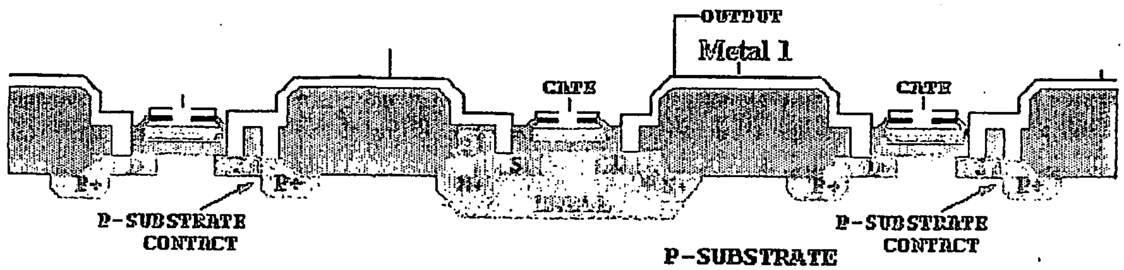
OUTPUT
Metal 1
GATE
GATE
P+
P-SUBSTRATE CONTACT
P-SUBSTRATE
P-SUBSTRATE CONTACT

FIG. 2

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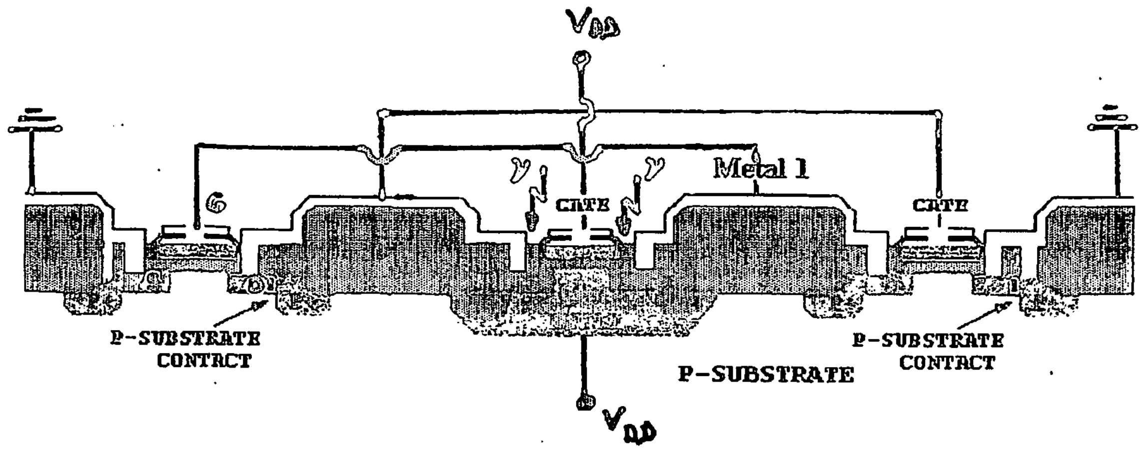

FIG. 2a

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/11 G11C11/412 H01L27/144

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4 675 715 A (SINHA ASHOK K ET AL) 23 June 1987 (1987-06-23) the whole document	1,4-6
Y	US 2003/039165 A1 (SHAU JENG-JYE) 27 February 2003 (2003-02-27) page 7, left-hand column, paragraph 0062 - paragraph '0063!; figures 8b-8e	1,4-6

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 February 2004	11/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Albrecht, C

International Application No
PCT/IB 03/01078

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	TAKATA H ET AL: "OPTICALLY COUPLED THREE-DIMENSIONAL COMMON MEMORY WITH NOVEL DATA TRANSFER METHOD" JAPANESE JOURNAL OF APPLIED PHYSICS, PUBLICATION OFFICE JAPANESE JOURNAL OF APPLIED PHYSICS. TOKYO, JP, 28 August 1989 (1989-08-28), pages 441-444, XP000087450 ISSN: 0021-4922 the whole document -----	1-3
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